Cape Peninsula University of Technology

F'SATI French South African Institute of Technology

Interface Control Document

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1 Document Control

Revision	Date	Section	Description
A	2015-11-10	All	First Release

2 Revision Control

Product	Part Number	Revisions Covered	Notes
CMC	CMC-01-00045	A	

3 Related Documents

No.	Document Name	Document Reference
OPT-01-00045	Options Sheet: CMC	Rev A
USM-01-00045	User Manual: CMC	Rev A

4 Nomenclature/Definitions

4.1 Abbreviations

BCD Binary coded decimal

CRC Cyclic redundancy check

FCS Frame check sequence

FPGA Field programmable gate array

TBC To be confirmed

TBD To be determined

PA Power amplifier

RSSI Received signal strength indicator

Rx Receive

SMPS Switched-mode power supply

SSID Secondary station identifier

Tx Transmit

5 Introduction

The transceiver is an integrated UHF-transmitter, VHF-receiver supporting both 9600 bps GMSK and 1200 bps AFSK. This document describes the mechanical, hardware and software interfaces between the transceiver and an OBC. A general overview of the intended operation for the transceiver is provided.

6 Overview

An overview of the transceiver is illustrated in Figure 1. The transceiver is a compact VHF/UHF Transceiver designed for CubeSat nanosatellite missions. It is compatible with the CubeSat nanosatellite standard, with a CubeSat Kit PC/104 form factor. The transceiver implements both 9600 bps GMSK and 1200 bps AFSK and operates in full-duplex mode with the options listed in Table 4.

The communication protocol implemented is AX.25 using unnumbered information (UI) packets. The transceiver also implements a transparent mode allowing the OBC to implement their own modulation scheme. CCSDS (1/2 Rate, K=7) encoding is available in transparent mode. All telemetry, commands and data are issued via I^2C. The transceiver operates as a slave on the I^2C bus and does not implement any pull-up resistors. The transmit frequency of the hardware has a range of 430–440 MHz. The frequency of operation is software selectable within the band and is adjustable in 25 kHz steps. The output power is adjustable from 27 to 33 dBm.

The receive frequency of the hardware has a range of 140–150 MHz. The frequency of operation is software selectable within the band and is adjustable in 12.5 kHz steps. The transceiver requires power from regulated 3.3 V and 5 V rails.

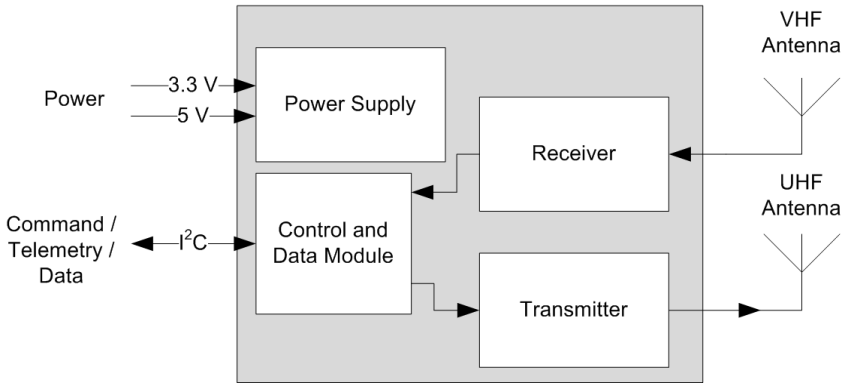

Figure 1: System block diagram

7 Absolute maximum ratings

Parameter	Notes	Value	Unit
Supply Voltage(s)	Regulated 5.0 V from bus	5.5	V
	Regulated 3.3 V from bus	4	V
Operating temperature		–25 to +61	°C
Storage Temperature		–40 to +85	°C

8 Electrical characteristics

Parameter	Notes	Min	Typ	Max	Unit
Power					
Voltage(s)	From a regulated 3.3 V bus	3.2	3.3	3.5	V
	From a regulated 5 V bus	4.7	5	5.5	V
Receiver only					
Current	From 3.3 V bus	-	64	-	mA
	From 5 V bus	-	<100	-	uA
Transmit only					
Current (from 5 V bus)	0.5 W (27 dBm) RF out	-	563	-	mA
	1 W (30 dBm) RF out	-	812	-	mA
	2 W (33 dBm) RF out	-	1202	-	A
DC Power					
Idle power	Receiver ON, transmitter OFF	-	211	-	mW
Transmit 0.5 W RF	Receiver ON, transmitter ON	-	3.0	-	W
Transmit 1 W RF	Receiver ON, transmitter ON	-	4.3	-	W
Transmit 2 W RF	Receiver ON, transmitter ON	-	6.2	-	W
RF characteristics					
Transmitter					
Frequency range		430	-	440	MHz
Output power		27	-	33	dBm
Spurious responses	10 MHz reference oscillator. 25 kHz comparison frequency.	-	<-65	-	dBc
Harmonic outputs		-	<-40	-	dBc
Frequency stability		-	±2.7	-	ppm
Frequency deviation		-	3	-	kHz
Channel spacing		-	25	-	kHz
Receiver					
Frequency range		140	-	150	MHz
Sensitivity	For 12 dB SINAD	-116	-117	-117	dBm
Dynamic range		-117	-	-70	dBm

Noise figure		-	<1.5	-	dB
Frequency stability		-	±2.7	-	ppm
Channel spacing		-	12.5	-	kHz
I^2C					
SCL frequency		50	400	500	kHz
Node address		-	0x25	-	hex
Address scheme		-	7	-	bit

9 Mechanical characteristics

Parameter	Notes	Min	Typ	Max	Unit
Physical					
Dimensions	See diagrams				
Weight		--	<100	--	g
Output ports					
RF connectors	Rx = SMA, Tx = SMA				

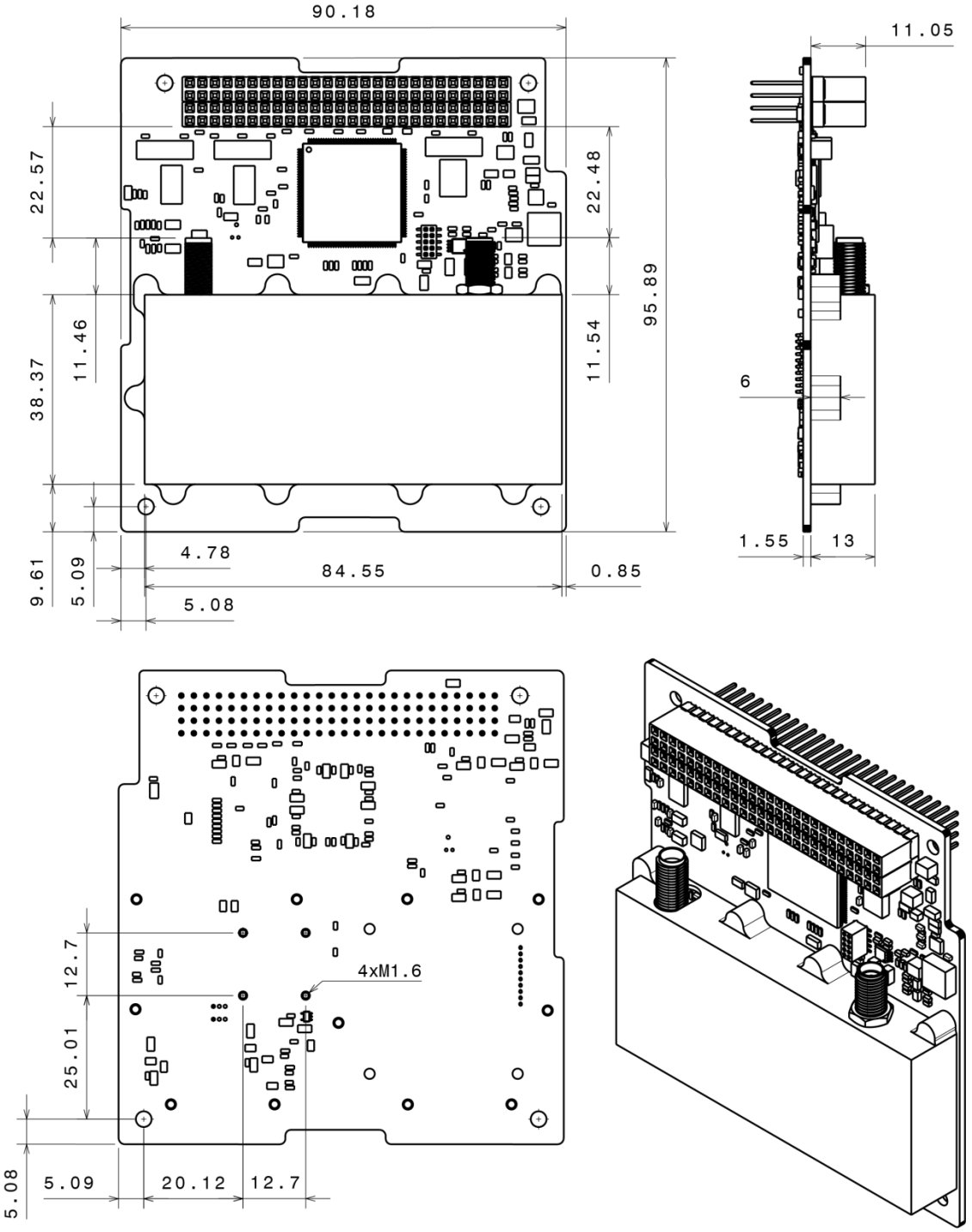

Figure 2: Mechanical diagrams (in mm)

10 Interfaces

10.1 Mechanical interfaces

10.1.1 Heat sink interface

Provision is made for a heat sink interface on the underside of the PCB. The RF enclosure provides four threaded pillars as depicted on the mechanical diagram which allow for M1.6 screws to fasten a heat sink to the unit. The thread in the pillars is approximately 3.2 mm deep. A simple L–shaped heat sink that attaches to the inside of the satellite structure is suggested. CHO-THERM® may be used between the board and the heat sink for improved thermal conductivity.

10.2 Hardware interfaces

10.2.1 CSK header connections

Figure 3 illustrates the connections that are made available at the CSK header. Broken lines indicate optional connections. The only non-optional connection to the header (excluding power signals) is I^2C. Optional connections that are provided on the header include DTMF signals, a transmit ready (TR) signal, transmit empty (TE), receive ready (RR), FPGA reset and the received baseband audio. The optional connections can be selected at the time of production and should be selected according to application and performance requirements. Should the optional functionality not be required it will not be made available at the header (there will be no physical connection). An explanation of the various connections is detailed later within this document. All signal voltage levels are 3.0 V LVCMOS. The AUDIO RX signal is the analogue demodulated baseband audio from the receiver. Note that should this signal be required that it is AC coupled meaning any DC offset would need to be recreated on the subsystem making use of the audio.

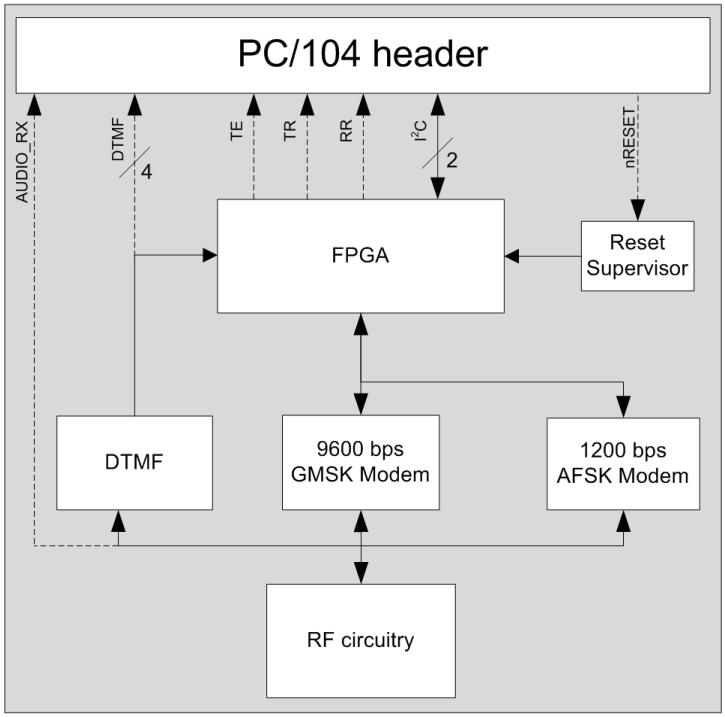

Figure 3: Block diagram of the CSK header connections. Broken lines indicate optional connections

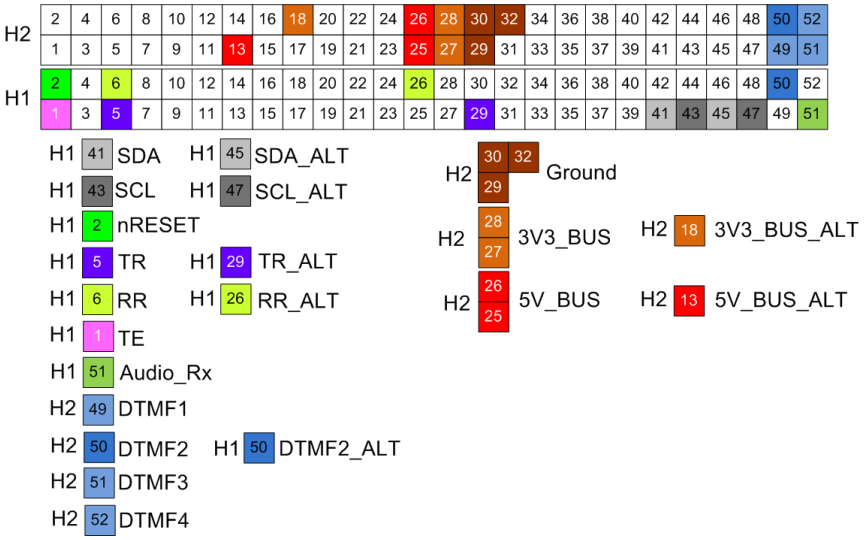

Figure 4: PC/104 header pinouts

Table 1: CSK connector pinouts

Signal name	Primary pin(s)	Alternate pin(s)	I/O type	Description	Optional
SDA	H1.41	H1.45	Bidirectional	I^2C serial data	No
SCL	H1.43	H1.47	Input	I^2C serial clock	No
nRESET	H1.2		Input	FPGA reset (active low)	Yes
TR	H1.5	H1.29	Output	Transmit ready	Yes
RR	H1.6	H1.26	Output	Receive ready	Yes
TE	H1.1		Output	Transmit empty	Yes
AUDIO_RX	H1.51		Output	Receiver baseband audio	Yes
DTMF1	H2.49		Output	Decoded DTMF signal 1	Yes
DTMF2	H2.50	H1.50	Output	Decoded DTMF signal 2	Yes
DTMF3	H2.51		Output	Decoded DTMF signal 3	Yes
DTMF4	H2.52		Output	Decoded DTMF signal 4	Yes
5V_BUS	H2.25, H2.26	H2.13	Power	5 V supply	No
3V3_BUS	H2.27, H2.28	H2.18	Power	3.3 V supply	No
GND	H2.29, H2.30, H2.32		Power	Power ground	No

10.2.2 FPGA reset

A reset signal is provided to the header that will allow an external subsystem such as an OBC to reset the FPGA to a known good state. This is an optional signal. Alternatively cycling the power of the radio or using the soft reset register will also place the FPGA into a known good state.

10.2.3 RF connectors

50 Ω SMA connectors will be used for RF receive and transmit. When connecting to the transceiver a right angle SMA connector should be used. When not transmitting into an antenna, ensure that an appropriate RF load is connected to prevent damaging the transmitter.

10.3 Software interfaces

10.3.1 AX.25

The AX.25 operates in a connectionless mode (Unnumbered Information (UI) frames). If on receipt a packet fails the CRC it will be dropped. The format of the AX.25 packet is illustrated in Table 2. It contains a fixed 16-byte header with a source (SRC), destination (DST) and SSID for each packet. The SRC and DST fields can be selected at time of production. An example of the DST field is “EARTH” and SRC field is “SPACE”. The data field can be anything from 1 byte to 256 bytes long. This is followed by the two-byte (16-bit) CRC.

Table 2: AX.25 packet format example. Column data values in hex. Values in brackets denote number of bytes per field

DST (6)	SSID (1)	SRC (6)	SSID (1)	Control (1)	PID (1)	Data (1-256)	FCS (2)
8a, 82, a4, a8, 90, 40	e0	a6, a0, 82, 86, 8a, 40	61	03	f0	...	...

10.3.2 Transparent Mode (Transmit only)

The transceiver can also operate in transparent mode (for transmit only). This is essentially a pass-through of the data directly to the modems, no protocol is implemented as this feature allows an OBC to implement its own. This feature is configurable via the transparent mode I^2C register. Additionally, a CCSDS 1/2 rate convolutional encoder K=7 (171 octal, 133 octal) can be enabled to encode the data. This feature is also configured in the transparent mode I^2C register. Do *not* implement the simple protocol framing method illustrated in Table 3 for transparent mode. The data is transmitted without any manipulation.

10.3.3 I²C operation

All data, telecommands and telemetry are communicated via I^2C. The default I^2C address is 0x25, but can be configured according to user specifications at time of production. Issuing a telecommand (writing data) has the following procedure. The first byte written to the I^2C points to the address of the register, and the following bytes write the value to the register. Reading telemetry follows a similar approach, firstly a byte is written to point to the correct register followed by a read transaction to return the value. Consecutive read transactions automatically increment the read pointer, except for a few registers (Refer to User Manual).

10.3.4 Operation

On power-up the transceiver is ready to receive and transmit data. It will boot up with the default settings for the modem, RF power setting, etc. As soon as data is available in the transmit buffer it is sent. Received data is also buffered to be retrieved over I^2C. The transceiver is optimally tuned for a 2 MHz band around the selected centre frequency (best receiver sensitivity and transmit power).

10.3.4.1 Transmit in AX.25 mode

Data to be transmitted is sent via an I^2C command. The format of the I^2C instruction will include the pointer to the data register followed by the data itself. The data must also follow a particular format. A simple protocol is implemented (Table 3) consisting of a two-byte preamble with the byte sequence 0x1A, 0xCF, followed by a single byte containing the length of the data, followed by the data itself and finally a checksum byte. The checksum is a summation of the values of the data bytes ignoring overflow. The length byte can indicate a data field length up to 256 bytes. In order to do this a value of 0 in the length field represents a data field length of 1, and 255 a data field length of 256 bytes respectively.

Table 3: Simple protocol for transmit data. Values in brackets indicate number of bytes

Preamble	Length	Data	Checksum

(2)		(1)	(1-256)	(1)
0x1A	0xCF	0x..	{ 0x..; ... ; 0x.. }	0x..

All of this information (preamble, length, data and checksum) is buffered in the transmit buffer. The size of the transmit buffer has been set to 4 kB (4096 bytes). Before writing data to the radio, a transmit buffer check should be performed to check the status of the buffer to see whether there is space for the data. A buffer status telemetry channel is provided to give an indication of the number of free byte slots available in the buffer. Data can be added to the buffer as long as there is space and should preferably be done as complete packets. This means that a number of smaller packets may be written to the buffer. Writes to the buffer when it is full are ignored. As the FPGA packages the AX.25 packet, the data in the buffer is searched sequentially for the preamble after which the number of bytes stipulated in the length field are packaged as AX.25 data. AX.25 data only includes bytes in the data field of the simple protocol. Data will only be packaged as AX.25 data if the simple protocol checksum passes.

A transmit ready (TR) flag is provided to the PC/104 header as a hard signal as well as via an I^2C telemetry channel as a soft signal. The hard TR signal should provide a performance advantage as opposed to polling the I^2C telemetry channel since it can be used to interrupt an OBC. The TR flag will become active once the number of bytes in the buffer drops below a predefined threshold indicating more data can be added to the buffer. The threshold trigger for the TR flag has been configured to 260 bytes. A transmit empty (TE) flag is also provided to the PC/104 header to indicate when the transmit buffer is empty. The TE signal is logic high when the transmit buffer is empty.

10.3.4.2 Transmit in transparent mode

In transparent mode the simple protocol mentioned above must not be implemented. Data is transmitted as soon as it is buffered. Sync bytes are transmitted while the RF circuitry is being powered or while there is no data in the buffer. If the transmit buffer is not continuously supplied with data the transmitter will automatically turn off after one second.

10.3.4.3 Sync bytes

Each individual AX.25 packet or the first packet of a sequence of AX.25 packets are preceded by a period of transmitting sync bytes. The minimum number of sync bytes preceding a transmission is configurable in a telecommand register. The hex value of the sync byte is 0x55. The purpose of the sync period is to provide the ground (receive) segment an opportunity to perform clock recovery from the signal and synchronise with the transmitter. A similar procedure should be observed when sending telecommands from the ground. Each AX.25 packet also includes a configurable number of AX.25 flags. The value of the AX.25 flag is 0x7E. If there are a number of AX.25 packets buffered in order to be transmitted then only the first packet will be preceded by sync bytes. Each AX.25 packet is however preceded by the configured number of AX.25 flags and terminated with a single flag. Sync bytes are transmitted while there is no data in the transmit buffer and the PTT is still keyed. Once the last packet has been sent and there is no more data in the buffer then PTT will be released.

10.3.4.4 Receive

On receiving telecommands from the ground, if the received AX.25 packet passes the CRC then the AX.25 data field is extracted, the simple protocol header and tail added and then buffered in the receive buffer. Each AX.25 packet must be preceded by at least one flag and terminated with at least one flag. Single flag sharing between packets is not supported. The size of the receive buffer is 4 kB (4096 bytes). As soon as data is available, the RR flag will become active, indicating data is ready to be retrieved. The RR flag is made available as an optional hard signal to the PC/104 header as well as a telemetry channel accessible over I^2C. The hard RR signal should provide a performance advantage as opposed to polling the I^2C telemetry channel since it can be used to interrupt an OBC. An additional I^2C telemetry channel must then be read to indicate how many bytes should be retrieved from the receive buffer. A value of zero for this telemetry channel indicates there is no data available. Any reads from the receive buffer when there is no data available will return a value of 0xff.

10.3.4.5 Full-duplex operation

The radio operates in full-duplex mode with the available configurable modes listed in Table 4. These modes are selectable as an I^2C command. If a reset occurs, then the default mode will be selected. A default mode can be requested at time of production.

Table 4: List of configurable modulation schemes and data rates for downlink/uplink

Configuration mode	Downlink / Uplink	Modulation scheme	Data rate (bps)
1 (default)	Downlink	GMSK	9600
	Uplink	AFSK	1200
2	Downlink	AFSK	1200
	Uplink	GMSK	9600
3	Downlink	GMSK	9600
	Uplink	GMSK	9600

10.3.5 Inactivity beacon

After a period of inactivity on the I^2C bus, configurable between 1 and 7 minutes, a Watchdog timer will overflow resulting in the transmission of a beacon message. The format of the data transmitted depends on the current state of the transmit register. If the transceiver is in AX.25 mode then the data will be formatted as an AX.25 packet. If transparent mode is selected then the raw data will get transmitted, possibly with encoding if that is selected. Another timer can be configured to set the period of delay between consecutive beacons, configurable between 10 and 127 seconds. The beacon message consists of local subsystem telemetry and a configurable 128 volatile bytes for user data. Any I^2C bus activity will reset the Watchdog and beacon operation. The beacon is enabled by default at time of production. It can be enabled/disabled through an I^2C command, however if a reset occurs then the default setting will return. The beacon does not perform any battery voltage measurements to determine whether it should stop beaconing.

The format of the transmitted beacon is presented in Table 5. A detailed description of the beacon I^2C registers can be found in the user manual. Registers are available to write, clear and enable the beacon, as well as to configure the timeout period.

Table 5: Inactivity beacon telemetry format

Telemetry	Bytes
Rx packet counter	2
RSSI	2
SMPS temperature	1
PA temperature	1
3V3 Current	2
3V3 Voltage	2
5 V Current	2
5 V Voltage	2
Custom message	128

10.3.6 DTMF backdoor

A DTMF backdoor has been implemented as a means to provide low level commands to the PC/104 connector via the transceiver in the event that ordinary communications are not responding or as a simple, direct command. Typical applications could allow an OBC to reset a subsystem.

The output of the DTMF receiver is provided directly to the PC/104 connector allowing another subsystem, such as an OBC, to interpret the low level decoded signals and perform a function. The current output of the DTMF receiver is also mimicked in a register on the FPGA that is accessible over I^2C. The decoded signals output by the DTMF receiver for a given tone are represented in Table 6.

Take note that the DTMF receiver will latch the digital representation of the last tone pair received and only until a new tone arrives will the latched output change. Since the outputs remain fixed (latched), two same tones must not be sent consecutively .i.e. if two 7's are sent consecutively the outputs from the DTMF receiver will not change as the digital representation of the tone is the same.

Table 6: Tone decoding

Digit	DTMF4	DTMF3	DTMF2	DTMF1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

10.3.7 Forward and reverse power

Included in the I^2C telemetry is the inclusion of a forward and reverse power registers. These registers allow for the calculation of the forward and reverse RF transmit power as well as return loss. This telemetry will provide an indication of the match between the transmitter and the antenna.